**Cell Description:**This is a standard TIEHI cell. The purpose of this cell is to hardcode a logic high signal. It is described by the following Boolean equation.

**Truth Table:**

|  |
| --- |
| **Y** |
| 1 |

**Behavioral Verilog:**

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| TIEHI | 27.0 | 4.8 |

**Logic Symbol:**

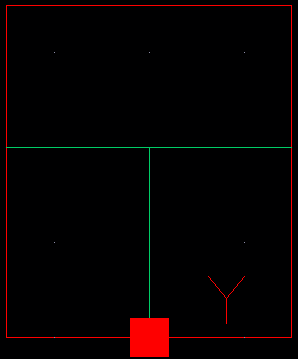
****

Figure 1: Symbol View for the TIEHI cell.

**CMOS Schematic:**

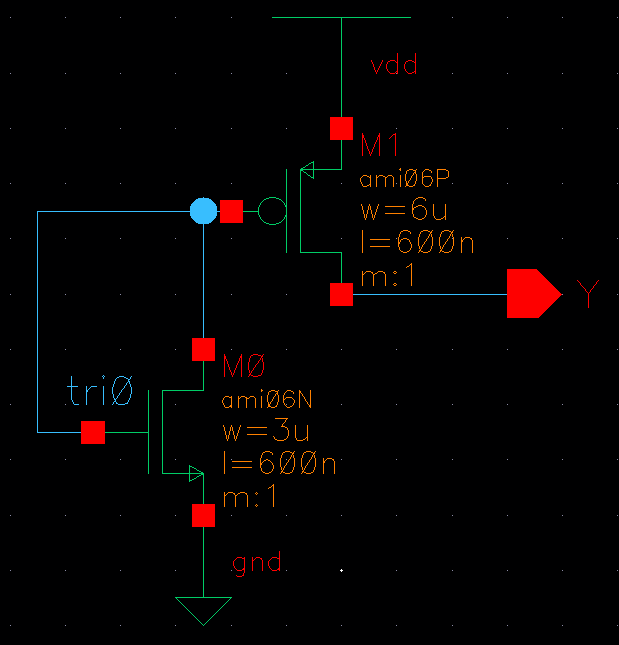
****

Figure 2: CMOS Schematic for the TIEHI cell.

**CMOS Layout:**

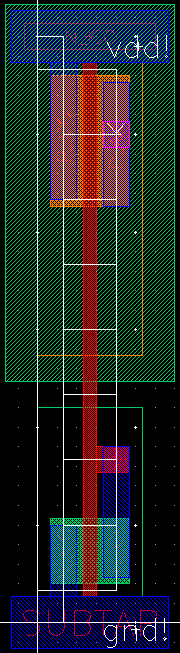
****

Figure 3: CMOS layout for the TIEHI cell